REMARKS

This Amendment and Reply seeks to place this application in better condition for allowance. All of the claims have been amended to correct inadvertent typographical errors, to improve grammar, clarity and/or antecedent basis, and/or to more fully protect the Applicants' invention(s). None of these amendments were motivated by patentability considerations in view of the prior art, including the art presented or cited during the prosecution of this application. No new matter has been added.

All of the objections and rejections raised in the Office Action of November 10, 2004 have been addressed. Each of the objections and rejections is addressed below in detail and in the order presented in the Office Action.

OFFICE ACTION

In the Office Action of November 10, 2004 (hereinafter the "Office Action"), the Examiner rejected claim 11 as being indefinite, and claims 1-3 and 10-14 as being anticipated by Burnett et al. (U.S. Patent 6,714,436). The remaining claims were found to contain patentable subject matter but were objected to as being dependent upon a rejected base claim.

All of the objections and rejections raised in the Office Action have been addressed herein. Each of the objections and rejections are addressed below in detail and in the order presented in the Office Action.

Rejection of Claim 11 under 35 USC §112

Claim 11 was rejected for lack of antecedent basis. In this regard, the phrase "the first gate line" had no antecedent basis. Applicants have corrected claim 11.

Notably, all of the claims have been reviewed and, where appropriate, amended to correct inadvertent typographical errors, and to improve grammar, clarity and/or antecedent basis. No new matter has been added. Moreover, none of these amendments were motivated by patentability considerations in view of the prior art, including the art presented or cited during the prosecution of this application.

Rejection of the Claims under 35 USC §102(e)

In the Office Action, claims 1-3 and 10-14 were rejected as being anticipated by Burnett et al., U.S. Patent 6,714,436 (hereinafter, "Burnett"). Applicants respectfully disagree that Burnett anticipates or renders obvious the inventions as claimed. The layout of the Burnett memory array is entirely different than the layout and/or architecture of the claimed invention. In this regard, Burnett describes and illustrates a memory array consisting of a plurality of electrically floating body transistor memory cells arranged in a layout and/or architecture whereby each memory cell of a row of memory cells of the array is connected to a different source line. In contrast, the claimed inventions include, among other things, a row of memory cells, wherein each memory cell of the row includes an electrically floating body transistor whose source region is connected to the same source line. (see, for example, independent claim 1). For at least that reason, the Burnett memory cell array neither teaches, suggests nor motivates one skilled in the art to implement the layout and/or architecture of the memory cell array as claimed in the instant application.

Notably, the reasons set forth below are *not* the only reasons the inventions of the independent claims are patentable over Burnett, either alone or in combination with other art (whether such art is of record or not). As such, no inference or conclusion should be

drawn that Applicants' response to this rejection is exhaustive; rather, for the sake of brevity, the remarks focus on some of the patentable aspects of the independent claims.

Burnett et al. (U.S. Patent 6,714,436)

Burnett describes a single-transistor capacitorless memory cell array. (See, Col. 3, lines 41-44). The transistors of Burnett memory cells include floating or isolated body regions that are programmed by modulating the threshold voltage of the transistor. (Col. 3, lines 45-47).

The transistors are arranged in an array of rows and columns. (Col. 5, lines 52-53 and Figure 2). For example, the Burnett array includes row 41, having memory cells 411 and 412 (among others which are not illustrated), and row 42, including memory cells 421 and 422 (among others which are not illustrated). (Col. 5, lines 52 to Col. 6, line 29; and Figure 4). In addition, the Burnett array

> includes a first word line 451 that is sequentially coupled to the gate conductors of cell 411 and cell 412, as well as the gate conductors of the remaining cells (not show) that constitute row 41. A second word line 452 is likewise sequentially coupled to the gate conductors of cell 421 and cell 422, as well as to the gate conductors of the remaining cells (not shown) that constitute row 42. (Col. 5, line 66 to Col. 6, line 6).

Notably, Burnett describes and illustrates that the source regions of the memory cells in a row of memory cells are connected to *different* source lines. In this regard, the source regions of the transistors of memory cells 411 and 412 (which correspond to row 41) are connected to source lines 471 and 472, respectively. Further, the source regions of the memory cells 421 and 422 (which correspond to row 41) are connected to source

lines 471 and 472, respectively. (See, FIGURES 1, 2 and 4, Col. 4, lines 25-28 and Col. 6, lines 13-20).

Thus, the Burnett array includes a layout or architecture whereby the transistors that comprise each row of memory cells are connected to different source lines.

Claimed Inventions

There are many inventions described in the instant application. In an effort to present a more concise response, the discussion below will focus on only certain aspects or features of the claimed inventions. As mentioned above, this response is not exhaustive; however, for the sake of brevity, these remarks focus on only some of the patentable features of the independent claims.

Independent Claim 1

Independent claim 1 describes a semiconductor memory array comprising a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns. Each semiconductor dynamic random access memory cell includes at least one transistor having, a source region, a drain region, and a body region disposed between the source region and the drain region, wherein the body region is electrically floating. The transistor also includes a gate spaced apart from, and capacitively coupled to, the body region.

Each memory cell includes (1) a first data state which corresponds to a first charge in the body region of the transistor of the memory cell, and (2) a second data state which corresponds to a second charge in the body region of the transistor of the memory cell.

Independent claim 1 further describes the source region of the transistor of each memory cell corresponding to a first row of semiconductor dynamic random access

memory cells is connected to the same source line. In addition, the gate of each memory cell corresponding to the first row of semiconductor dynamic random access memory cells is connected to the same word line.

Independent Claim 12

Independent claim 12 describes a semiconductor memory array comprising a plurality of semiconductor dynamic random access memory cells arranged in a matrix of rows and columns. Each semiconductor dynamic random access memory cell includes at least one transistor having, a source region, a drain region, and a body region disposed between the source region and the drain region, wherein the body region is electrically floating. The transistor also includes a gate spaced apart from, and capacitively coupled to, the body region.

Each memory cell includes (1) a first data state which corresponds to a first charge in the body region of the transistor of the memory cell, and (2) a second data state which corresponds to a second charge in the body region of the transistor of the memory cell.

Independent claim 12 further describes the source region of the transistor of each memory cell corresponding to a first row of semiconductor dynamic random access memory cells is connected to a first source line; and the gate of the transistor of each memory cell corresponding to the first row of semiconductor dynamic random access memory cells is connected to a first word line. In addition, the source region of the transistor of each memory cell corresponding to a second row of semiconductor dynamic random access memory cells is connected to a second source line; and the gate of the transistor of each memory cell corresponding to the second row of semiconductor dynamic random access memory cells is connected to a second word line. Independent claim 12

defines the first and second rows of semiconductor dynamic random access memory cells as adjacent rows.

Burnett Does NOT Anticipate or Render Obvious the Claimed Inventions

Simply put, Burnett neither anticipates nor renders obvious the claimed invention. In this regard, Burnett does not teach or suggest a memory array including a row of memory cells (each memory cell comprised of electrically floating body transistor) whereby the source regions of the transistors are connected to the *same* source line. Rather, Burnett teaches the opposite – that is, the source regions of the transistors of the memory cells of a given row are connected to *different* source lines. As such, the Burnett memory array, among other things, does not teach, suggest or motivate one skilled in the art to provide a common source line for each row of memory cells of the memory array.

Moreover, there is absolutely no suggestion or motivation to one skilled in the art to implement the layout of the claimed invention. That is, there is no suggestion or motivation to one skilled in the art to connect the same source line to the source regions of the transistor of the memory cells of a given row. Indeed, such an arrangement would likely require a dramatic alteration of the layout of the Burnett memory array. In this regard, the source lines SL18 would likely extend in a direction that is perpendicular to the bit lines BL17 rather than parallel to the bit lines BL17 as described and illustrated in Burnett. (See, for example, FIGURE 2 and Col. 4, lines 49-64). Moreover, such a change would likely require the source lines SL18 to extend in a direction that is parallel to the word lines WL16 rather than parallel to the word lines WL 16 as described and illustrated in Burnett. (See, for example, FIGURE 2 and Col. 4, lines 49-64).

In sum, Burnett, alone or in combination with other prior art, does not anticipate or render obvious the claimed inventions.

Dependent Claims

Several of the dependent claims have already been found to include patentable subject matter. As for the rejected dependent claims, for the sake of brevity, the additional reasons/bases that those dependent claims are patentable over Burnett are not set forth herein. However, for at least the reasons stated above, it is respectfully submitted that such rejected dependent claims are patentable in view of Burnett.

Statement of Reasons for the Indication of Allowable Subject Matter

Many of the claims were found to contain patentable subject matter in the initial Action. No inference or conclusion should be drawn that Applicants believe that the Examiner's reasons for allowance are the *only* reasons those claims are patentable. For the sake of brevity, the additional reasons/bases that those dependent claims are patentable over Burnett are not set forth herein. Notably, it is the Applicants' position that such claims are also patentable for the same reasons expressed above.

Prior Art Made of Record

Applicants note the prior art made of record but not relied upon. It is not clear what is the relevance of (or meant by) the comment that the prior art made of record "is considered pertinent to applicant's disclosure." (See, Office Action, page 5). No inference or conclusion should be drawn that Applicants agree, in any way, with the Examiner's characterization of such prior art. In an effort to provide a more concise response, and

because the Examiner has not rejected any of the claims based on the prior art made of record, Applicants provide no comment on the Examiner's characterization.

Amendment to the Claims

As mentioned above, the claims have been amended to correct inadvertent typographical errors, improve grammar, clarity and/or antecedent basis, and to more fully protect the Applicants' invention(s). No new matter has been added.

Notably, none of the amendments were motivated by patentability considerations in view of the prior art, including the art relied on in the outstanding Office Action.

Information Disclosure Statements

Second and Fourth Information Disclosure Statements

Applicants submitted a Second Information Disclosure Statement ("IDS"), including Form PTO-1449, on August 11, 2004. A copy of the Second IDS (and Form PTO-1449) is attached hereto. The Second IDS was received by the USPTO on August 16, 2004. (See, Stamped Postcard).

Applicants submitted a Fourth IDS, including Form PTO-1449, on August 12, 2004. A copy of the Fourth IDS (and Form PTO-1449) is attached hereto. The Fourth IDS was received by the USPTO on August 16, 2004. (See, Stamped Postcard).

The Office Action did not include an indication that the Second IDS and Fourth IDS were considered by the Examiner. As such, it is again respectfully requested that the Examiner make his/her consideration of the references identified in each IDS formally of record with the next action.

CONCLUSION

Applicants respectfully request entry of the foregoing amendments and reconsideration of the instant application. Applicants submit that all of the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

It is noted that should a telephone interview expedite the prosecution of this application in any way, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: November 19, 2004

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